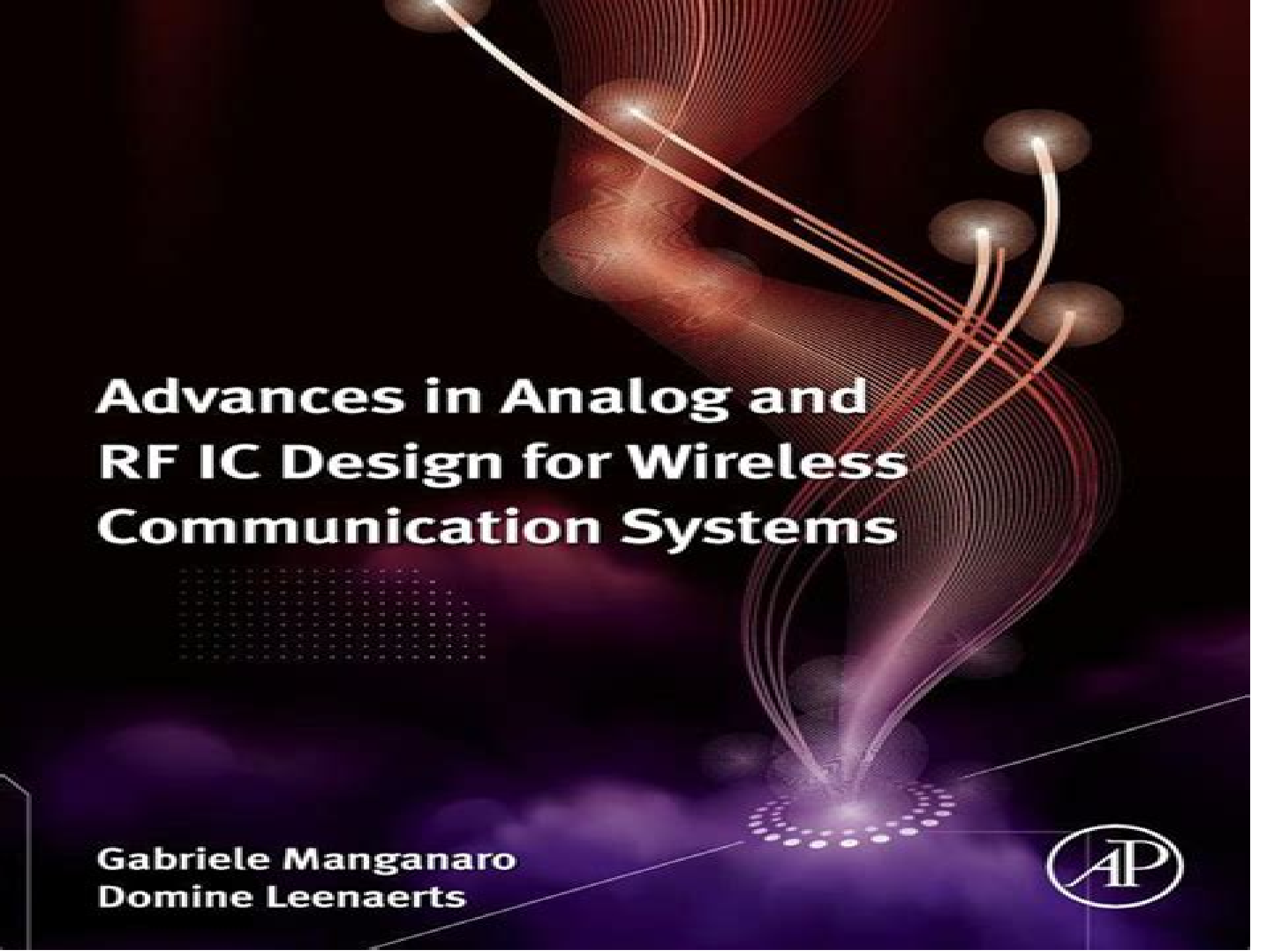




Advances in Analog and RF IC Design for Wireless Communication Systems

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**Gabriele Manganaro
Domine Leenaerts**



Advances In Analog And Rf Ic Design For Wireless Communication Systems

Gil Engel, Gabriele Manganaro



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Advances in Analog and RF IC Design for Wireless Communication Systems Pascal Philippe, Louis Praamsma, Marcel Geurts, 2013-05-13 This chapter presents one of the first integrated Ku band downconverters with PLL frequency synthesizer that has widely penetrated the market of low noise blocks LNBs for reception of satellite television It starts with a brief description of the general architecture of a LNB and a presentation of the main requirements for the integrated downconverter and frequency synthesizer The architecture of the integrated circuit and the design of its building blocks are then presented and discussed in detail The emphasis is put on the design choices made in the downconverter and

the synthesizer for competing in cost and performance with discrete implementations at minimal power consumption By the end of the chapter measurement results are reported that illustrate the downconverter performance alone or within a demonstration LNB

Advances in Analog and RF IC Design for Wireless Communication Systems Mustafa Acar, Mark P. van der Heijden, Jawad H. Qureshi, 2013-05-13 This chapter presents high efficiency power amplifiers PAs for wireless infrastructure It starts by stating the importance of high efficiency and the historical evolution in base station PA concepts It then introduces the current solution the Doherty PA After explaining the fundamentals of the Doherty PA a novel implementation achieving more than 35% drain efficiency across a 6dB power back off range and up to 20W peak power between 1.7 and 2.3GHz is given Afterwards a future PA concept switch mode outphasing PA is introduced Theory and implementation details of a class E outphasing PA achieving more than 60% drain efficiency across a 6dB power back off range and up to 19W peak power between 1800 and 2050MHz is explained By the end of the chapter an essential part of switch mode PAs high voltage up to 10V and high frequency up to 4GHz drivers are presented

Advances in Analog and RF IC Design for Wireless Communication Systems Gil Engel, Gabriele Manganaro, 2013-05-13 This chapter discusses the practical application of RF digital to analog converters RF DACs to communication systems such as cable distribution wireless communications infrastructure WIFR base stations wireless backhaul and other such systems The key specifications that are driving the development of RF DAC technology are reviewed as are some common radio architectures used to implement those systems Challenges associated with the design of RF DACs are described and some trade offs and possible solutions are discussed Design considerations of the package and the printed circuit board PCB design are reviewed Measured results of an RF DAC suitable for cable head end transmitters are presented The features and performance of RF DACs provide an enabling solution for Software Defined Radio SDR systems targeted toward multi carrier multi band multi standard radio transmitters

Advances in Analog and RF IC Design for Wireless Communication Systems Hooman Darabi, 2013-05-13 This chapter offers a system level analysis of advanced RF transceivers intended for use in wireless and particularly mobile applications An overview of RF cellular standards is presented followed by a discussion of various radio architectures The key radio requirements are derived and translated to circuit specs giving an overview of a practical top down radio design Several radio non idealities resulting from RF CMOS shortcomings are discussed and various architectural and calibration techniques are introduced to overcome those We will also cover more advanced topics such as handset calibration the evolution to broadband RF diversity and next generation mobile standards and their requirements

Advances in Analog and RF IC Design for Wireless Communication Systems Domine Leenaerts, 2013-05-13 Radios for cellular wireless infrastructure require low noise amplifiers LNAs with very demanding requirements on noise and linearity performance So far these amplifiers have been realized in III V technologies but for various reasons silicon based LNAs are needed too This chapter will explain the challenges in LNA design for this application field

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and RF IC Design for Wireless Communication Systems Richard Schreier,Hajime Shibata,2013-05-13 Design concepts and an example of bandpass Delta Sigma ADCs for wireless receivers are described Delta Sigma ADC design involves a variety of choices in the system design phase such as lowpass vs bandpass loop filter or feedback vs feedforward architecture In the first half of the chapter such system decisions are compared and discussed in the context of wireless communication applications The latter half of the Chapter describes an example bandpass Delta Sigma ADC design based on the aforementioned discussions Circuit implementations and measurement results are disclosed in details Advances in Analog and RF IC Design for Wireless Communication Systems Michael Elliott,Boris Murmann,2013-05-13 This chapter provides an overview of design techniques and system aspects relevant to the application of high speed pipelined ADCs in wireless base transceiver stations BTS The discussion begins with a derivation of typical ADC specifications for the receive path of a multi carrier BTS system Next we investigate issues pertaining to the interface between the ADC and its driving circuitry including complications that arise with sample and hold amplifier less SHA less ADC frontends Lastly we summarize recent research results that look into the digital linearization of dynamic nonlinearities at the ADC s frontend **Advances in Analog and RF IC Design for Wireless Communication Systems** Salvatore Levantino,Carlo Samori,2013-05-13 In less than one decade after their introduction into radio frequency applications digital fractional N phase locked loops PLLs have become a relevant topic in microelectronic research and a practical solution for products In addition to the well known advantages such as their silicon area occupation scaling as technology node and their easier portability to new nodes digital PLLs enable easy and low cost implementation of calibration techniques which substantially reduce spurious tones and remove other major analog impairments In wideband PLLs the ultimate level of spur performance is often bounded by the time resolution and the linearity of the time to digital converter within the digital PLL Methods for mitigating its nonlinearity such as those based on element randomization and large scale dithering are discussed The use of fractional N dividers based on digital to time converters as a means to relax the design of the time to digital converter is also reviewed This concept is extended to the limit case of a single bit time to digital converter which provides best PLL noise power trade off with good spur performance

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