

Parag K. Lala

An Introduction to Logic Circuit Testing

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Brendan G. Carr



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Digital Circuit Testing Francis C. Wong, 2012-12-02 Recent technological advances have created a testing crisis in the electronics industry smaller more highly integrated electronic circuits and new packaging techniques make it increasingly difficult to physically access test nodes New testing methods are needed for the next generation of electronic equipment and a great deal of emphasis is being placed on the development of these methods Some of the techniques now becoming popular include design for testability DFT built in self test BIST and automatic test vector generation ATVG This book will provide a practical introduction to these and other testing techniques For each technique introduced the author provides real world examples so the reader can achieve a working knowledge of how to choose and apply these increasingly important testing methods

High Performance Integer Arithmetic Circuit Design on FPGA Ayan Palchoudhuri, Rajat Subhra Chakraborty, 2015-07-06 This book describes the optimized implementations of

several arithmetic datapath controlpath and pseudorandom sequence generator circuits for realization of high performance arithmetic circuits targeted towards a specific family of the high end Field Programmable Gate Arrays FPGAs It explores regular modular cascadable and bit sliced architectures of these circuits by directly instantiating the target FPGA specific primitives in the HDL Every proposed architecture is justified with detailed mathematical analyses Simultaneously constrained placement of the circuit building blocks is performed by placing the logically related hardware primitives in close proximity to one another by supplying relevant placement constraints in the Xilinx proprietary User Constraints File The book covers the implementation of a GUI based CAD tool named FlexiCore integrated with the Xilinx Integrated Software Environment ISE for design automation of platform specific high performance arithmetic circuits from user level specifications This tool has been used to implement the proposed circuits as well as hardware implementations of integer arithmetic algorithms where several of the proposed circuits are used as building blocks Implementation results demonstrate higher performance and superior operand width scalability for the proposed circuits with respect to implementations derived through other existing approaches This book will prove useful to researchers students and professionals engaged in the domain of FPGA circuit optimization and implementation

Timing Performance of Nanometer Digital Circuits Under Process Variations Victor Champac, Jose Garcia Gervacio, 2018-04-18 This book discusses the digital design of integrated circuits under process variations with a focus on design time solutions The authors describe a step by step methodology going from logic gates to logic paths to the circuit level Topics are presented in comprehensively without overwhelming use of analytical formulations Emphasis is placed on providing digital designers with understanding of the sources of process variations their impact on circuit performance and tools for improving their designs to comply with product specifications Various circuit level design hints are highlighted so that readers can use then to improve their designs A special treatment is devoted to unique design issues and the impact of process variations on the performance of FinFET based circuits This book enables readers to make optimal decisions at design time toward more efficient circuits with better yield and higher reliability

Integrated Circuit Test Engineering Ian A. Grout, 2005-08-22 Using the book and the software provided with it the reader can build his her own tester arrangement to investigate key aspects of analog digital and mixed system circuits Plan of attack based on traditional testing circuit design and circuit manufacture allows the reader to appreciate a testing regime from the point of view of all the participating interests Worked examples based on theoretical bookwork practical experimentation and simulation exercises teach the reader how to test circuits thoroughly and effectively

Network and Parallel Computing James J. Park, Albert Y. Zomaya, Sang-Soo Yeo, Sartaj Sahni, 2012-12-09 This book constitutes the refereed post proceedings of the 9th IFIP International Conference on Network and Parallel Computing NPC 2012 held in Gwangju Korea in September 2012 The 38 papers presented were carefully reviewed and selected from 136 submissions The papers are organized in the following topical sections algorithms scheduling analysis and data mining network architecture and

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