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# Automatic Parallelization

*An Overview of Fundamental  
Compiler Techniques*

Samuel P. Midkiff

*SYNTHESIS LECTURES ON  
COMPUTER ARCHITECTURE*

Mark D. Hill, *Series Editor*

# Automatic Parallelization An Overview Of Fundamental Compiler Techniques Samuel P Midkiff

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## **Automatic Parallelization An Overview Of Fundamental Compiler Techniques Samuel P Midkiff:**

Automatic Parallelization Samuel Midkiff,2012-01-01 Compiling for parallelism is a longstanding topic of compiler research This book describes the fundamental principles of compiling regular numerical programs for parallelism We begin with an explanation of analyses that allow a compiler to understand the interaction of data reads and writes in different statements and loop iterations during program execution These analyses include dependence analysis use def analysis and pointer analysis Next we describe how the results of these analyses are used to enable transformations that make loops more amenable to parallelization and discuss transformations that expose parallelism to target shared memory multicore and vector processors We then discuss some problems that arise when parallelizing programs for execution on distributed memory machines Finally we conclude with an overview of solving Diophantine equations and suggestions for further readings in the topics of this book to enable the interested reader to delve deeper into the field Table of Contents Introduction and overview Dependence analysis dependence graphs and alias analysis Program parallelization Transformations to modify and eliminate dependences Transformation of iterative and recursive constructs Compiling for distributed memory machines Solving Diophantine equations A guide to further reading *Automatic Parallelization* Samuel Midkiff,2022-06-01 Compiling for parallelism is a longstanding topic of compiler research This book describes the fundamental principles of compiling regular numerical programs for parallelism We begin with an explanation of analyses that allow a compiler to understand the interaction of data reads and writes in different statements and loop iterations during program execution These analyses include dependence analysis use def analysis and pointer analysis Next we describe how the results of these analyses are used to enable transformations that make loops more amenable to parallelization and discuss transformations that expose parallelism to target shared memory multicore and vector processors We then discuss some problems that arise when parallelizing programs for execution on distributed memory machines Finally we conclude with an overview of solving Diophantine equations and suggestions for further readings in the topics of this book to enable the interested reader to delve deeper into the field Table of Contents Introduction and overview Dependence analysis dependence graphs and alias analysis Program parallelization Transformations to modify and eliminate dependences Transformation of iterative and recursive constructs Compiling for distributed memory machines Solving Diophantine equations A guide to further reading **Parallel Processing, 1980 to 2020** Robert Kuhn,David Padua,2022-05-31 This historical survey of parallel processing from 1980 to 2020 is a follow up to the authors 1981 Tutorial on Parallel Processing which covered the state of the art in hardware programming languages and applications Here we cover the evolution of the field since 1980 in parallel computers ranging from the Cyber 205 to clusters now approaching an exaflop to multicore microprocessors and Graphic Processing Units GPUs in commodity personal devices parallel programming notations such as OpenMP MPI message passing and CUDA streaming notation and seven parallel applications such as finite element analysis

and computer vision Some things that looked like they would be major trends in 1981 such as big Single Instruction Multiple Data arrays disappeared for some time but have been revived recently in deep neural network processors There are now major trends that did not exist in 1980 such as GPUs distributed memory machines and parallel processing in nearly every commodity device This book is intended for those that already have some knowledge of parallel processing today and want to learn about the history of the three areas In parallel hardware every major parallel architecture type from 1980 has scaled up in performance and scaled out into commodity microprocessors and GPUs so that every personal and embedded device is a parallel processor There has been a confluence of parallel architecture types into hybrid parallel systems Much of the impetus for change has been Moore's Law but as clock speed increases have stopped and feature size decreases have slowed down there has been increased demand on parallel processing to continue performance gains In programming notations and compilers we observe that the roots of today's programming notations existed before 1980 And that through a great deal of research the most widely used programming notations today although the result of much broadening of these roots remain close to target system architectures allowing the programmer to almost explicitly use the target's parallelism to the best of their ability The parallel versions of applications directly or indirectly impact nearly everyone computer expert or not and parallelism has brought about major breakthroughs in numerous application areas Seven parallel applications are studied in this book

Deep Learning Systems Andres Rodriguez, 2022-05-31 This book describes deep learning systems the algorithms compilers and processor components to efficiently train and deploy deep learning models for commercial applications The exponential growth in computational power is slowing at a time when the amount of compute consumed by state of the art deep learning DL workloads is rapidly growing Model size serving latency and power constraints are a significant challenge in the deployment of DL models for many applications Therefore it is imperative to codesign algorithms compilers and hardware to accelerate advances in this field with holistic system level and algorithm solutions that improve performance power and efficiency Advancing DL systems generally involves three types of engineers 1 data scientists that utilize and develop DL algorithms in partnership with domain experts such as medical economic or climate scientists 2 hardware designers that develop specialized hardware to accelerate the components in the DL models and 3 performance and compiler engineers that optimize software to run more efficiently on a given hardware Hardware engineers should be aware of the characteristics and components of production and academic models likely to be adopted by industry to guide design decisions impacting future hardware Data scientists should be aware of deployment platform constraints when designing models Performance engineers should support optimizations across diverse models libraries and hardware targets The purpose of this book is to provide a solid understanding of 1 the design training and applications of DL algorithms in industry 2 the compiler techniques to map deep learning code to hardware targets and 3 the critical hardware features that accelerate DL systems This book aims to facilitate co innovation for the advancement of DL systems It is written for

engineers working in one or more of these areas who seek to understand the entire system stack in order to better collaborate with engineers working in other parts of the system stack The book details advancements and adoption of DL models in industry explains the training and deployment process describes the essential hardware architectural features needed for today's and future models and details advances in DL compilers to efficiently execute algorithms across various hardware targets Unique in this book is the holistic exposition of the entire DL system stack the emphasis on commercial applications and the practical techniques to design models and accelerate their performance The author is fortunate to work with hardware software data scientist and research teams across many high technology companies with hyperscale data centers These companies employ many of the examples and methods provided throughout the book

**Hardware and Software Support for Virtualization** Edouard Bugnion, Jason Nieh, Dan Tsafir, 2022-06-01 This book focuses on the core question of the necessary architectural support provided by hardware to efficiently run virtual machines and of the corresponding design of the hypervisors that run them Virtualization is still possible when the instruction set architecture lacks such support but the hypervisor remains more complex and must rely on additional techniques Despite the focus on architectural support in current architectures some historical perspective is necessary to appropriately frame the problem The first half of the book provides the historical perspective of the theoretical framework developed four decades ago by Popek and Goldberg It also describes earlier systems that enabled virtualization despite the lack of architectural support in hardware As is often the case theory defines a necessary but not sufficient set of features and modern architectures are the result of the combination of the theoretical framework with insights derived from practical systems The second half of the book describes state of the art support for virtualization in both x86 64 and ARM processors This book includes an in depth description of the CPU memory and I/O virtualization of these two processor architectures as well as case studies on the Linux KVM VMware and Xen hypervisors It concludes with a performance comparison of virtualization on current generation x86 and ARM based systems across multiple hypervisors

**A Primer on Memory Persistency** Vaibhav Gogte, Aasheesh Kolli, Thomas F.

Wenisch, 2022-02-09 This book introduces readers to emerging persistent memory PM technologies that promise the performance of dynamic random access memory DRAM with the durability of traditional storage media such as hard disks and solid state drives SSDs Persistent memories PMs such as Intel's Optane DC persistent memories are commercially available today Unlike traditional storage devices PMs can be accessed over a byte addressable load store interface with access latency that is comparable to DRAM Unfortunately existing hardware and software systems are ill equipped to fully avail the potential of these byte addressable memory technologies as they have been designed to access traditional storage media over a block based interface Several mechanisms have been explored in the research literature over the past decade to design hardware and software systems that provide high performance access to PMs Because PMs are durable they can retain data across failures such as power failures and program crashes Upon a failure recovery mechanisms may inspect PM

data reconstruct state and resume program execution Correct recovery of data requires that operations to the PM are properly ordered during normal program execution Memory persistency models define the order in which memory operations are performed at the PM Much like memory consistency models memory persistency models may be relaxed to improve application performance Several proposals have emerged recently to design memory persistency models for hardware and software systems and for high level programming languages These proposals differ in several key aspects they relax PM ordering constraints introduce varying programmability burden and introduce differing granularity of failure atomicity for PM operations This primer provides a detailed overview of the various classes of the memory persistency models their implementations in hardware programming languages and software systems proposed in the recent research literature and the PM ordering techniques employed by modern processors

**Die-stacking Architecture** Yuan Xie,Jishen Zhao,2022-05-31 The emerging three dimensional 3D chip architectures with their intrinsic capability of reducing the wire length promise attractive solutions to reduce the delay of interconnects in future microprocessors 3D memory stacking enables much higher memory bandwidth for future chip multiprocessor design mitigating the memory wall problem In addition heterogenous integration enabled by 3D technology can also result in innovative designs for future microprocessors This book first provides a brief introduction to this emerging technology and then presents a variety of approaches to designing future 3D microprocessor systems by leveraging the benefits of low latency high bandwidth and heterogeneous integration capability which are offered by 3D technology

**A Primer on Memory Consistency and Cache Coherence, Second Edition** Vijay Nagarajan,Daniel J. Sorin,Mark D. Hill,David A. Wood,2022-05-31 Many modern computer systems including homogeneous and heterogeneous architectures support shared memory in hardware In a shared memory system each of the processor cores may read and write to a single shared address space For a shared memory machine the memory consistency model defines the architecturally visible behavior of its memory system Consistency definitions provide rules about loads and stores or memory reads and writes and how they act upon memory As part of supporting a memory consistency model many machines also provide cache coherence protocols that ensure that multiple cached copies of data are kept up to date The goal of this primer is to provide readers with a basic understanding of consistency and coherence This understanding includes both the issues that must be solved as well as a variety of solutions We present both high level concepts as well as specific concrete examples from real world systems This second edition reflects a decade of advancements since the first edition and includes among other more modest changes two new chapters one on consistency and coherence for non CPU accelerators with a focus on GPUs and one that points to formal work and tools on consistency and coherence

**Compiling Algorithms for Heterogeneous Systems** Steven Bell,Jing Pu,James Hegarty,Mark Horowitz,2022-05-31 Most emerging applications in imaging and machine learning must perform immense amounts of computation while holding to strict limits on energy and power To meet these goals architects are building increasingly specialized compute engines tailored for these

specific tasks The resulting computer systems are heterogeneous containing multiple processing cores with wildly different execution models Unfortunately the cost of producing this specialized hardware and the software to control it is astronomical Moreover the task of porting algorithms to these heterogeneous machines typically requires that the algorithm be partitioned across the machine and rewritten for each specific architecture which is time consuming and prone to error Over the last several years the authors have approached this problem using domain specific languages DSLs high level programming languages customized for specific domains such as database manipulation machine learning or image processing By giving up generality these languages are able to provide high level abstractions to the developer while producing high performance output The purpose of this book is to spur the adoption and the creation of domain specific languages especially for the task of creating hardware designs In the first chapter a short historical journey explains the forces driving computer architecture today Chapter 2 describes the various methods for producing designs for accelerators outlining the push for more abstraction and the tools that enable designers to work at a higher conceptual level From there Chapter 3 provides a brief introduction to image processing algorithms and hardware design patterns for implementing them Chapters 4 and 5 describe and compare Darkroom and Halide two domain specific languages created for image processing that produce high performance designs for both FPGAs and CPUs from the same source code enabling rapid design cycles and quick porting of algorithms The final section describes how the DSL approach also simplifies the problem of interfacing between application code and the accelerator by generating the driver stack in addition to the accelerator configuration This book should serve as a useful introduction to domain specialized computing for computer architecture students and as a primer on domain specific languages and image processing hardware for those with more experience in the field

### **Datacenter Design and**

### **Management**

Benjamin C. Lee, 2022-05-31 An era of big data demands datacenters which house the computing infrastructure that translates raw data into valuable information This book defines datacenters broadly as large distributed systems that perform parallel computation for diverse users These systems exist in multiple forms private and public and are built at multiple scales Datacenter design and management is multifaceted requiring the simultaneous pursuit of multiple objectives Performance efficiency and fairness are first order design and management objectives which can each be viewed from several perspectives This book surveys datacenter research from a computer architect's perspective addressing challenges in applications design management server simulation and system simulation This perspective complements the rich bodies of work in datacenters as a warehouse scale system which study the implications for infrastructure that encloses computing equipment and in datacenters as distributed systems which employ abstract details in processor and memory subsystems This book is written for first or second year graduate students in computer architecture and may be helpful for those in computer systems The goal of this book is to prepare computer architects for datacenter oriented research by describing prevalent perspectives and the state of the art

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