

Kingshuk Karuri · Rainer Leupers

Application Analysis Tools for ASIP Design

Application Profiling and
Instruction-set Customization

Application Analysis Tools For Asip Design Application Profiling And Instruction Set Customization

Kingshuk Karuri,Rainer Leupers



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Application Analysis Tools for ASIP Design Kingshuk Karuri, Rainer Leupers, 2011-06-15 This book introduces a novel design methodology which can significantly reduce the ASIP development effort through high degrees of design automation. The key elements of this new design methodology are a powerful application profiler and an automated instruction set customization tool which considerably lighten the burden of mapping a target application to an ASIP architecture in the initial design stages. The book includes several design case studies with real life embedded applications to demonstrate how the methodology and the tools can be used in practice for accelerating the overall ASIP design process. Computational

Science and Computational Intelligence Hamid R. Arabnia, Leonidas Deligiannidis, Farzan Shenavarmasouleh, Soheyla Amirian, Farid Ghareh Mohammadi, 2025-09-12 This CCIS book constitutes selected papers accepted in the Research Track on Computational Science and the Research Track on Computational Intelligence held as part of the 11th International Conference on Computational Science and Computational Intelligence CSCI 2024 which took place in Las Vegas NV USA during December 11-13 2024. The 24 full papers included in this book were carefully reviewed and selected from a total of 78 submissions. The Research Track on Computational Science CSCI RTSC received 78 submissions of which 17 papers were accepted. 16 of these are included in this volume. For the Research Track on Computational Intelligence CSCI RTCI 10 papers were accepted from 59 submissions. The contributions were organized in topical sections on Computational Science Frameworks Applications and Algorithms Computational Science Mathematics Simulation Performance Studies Optimization and Programming and Computational Intelligence Optimization Applications and Algorithms. **Energy-Efficient**

Communication Processors Robert Fasthuber, Francky Catthoor, Praveen Raghavan, Frederik Naessens, 2013-05-29 This book describes a new design approach for energy efficient Domain Specific Instruction set Processor DSIP architectures for the wireless baseband domain. The innovative techniques presented enable co design of algorithms architectures and technology for efficient implementation of the most advanced technologies. To demonstrate the feasibility of the author's design approach case studies are included for crucial functionality of advanced wireless systems with increased computational performance flexibility and reusability. Designers using this approach will benefit from reduced development product costs and greater scalability to future process technology nodes. **Pipelined Multiprocessor System-on-Chip**

for Multimedia Haris Javaid, Sri Parameswaran, 2013-11-26 This book describes analytical models and estimation methods to enhance performance estimation of pipelined multiprocessor systems on chip MPSoCs. A framework is introduced for both design time and run time optimizations. For design space exploration several algorithms are presented to minimize the area footprint of a pipelined MPSoC under a latency or a throughput constraint. A novel adaptive pipelined MPSoC architecture is described where idle processors are transitioned into low power states at run time to reduce energy consumption. Multi mode pipelined MPSoCs are introduced where multiple pipelined MPSoCs optimized separately are merged into a single pipelined

MPSoC enabling further reduction of the area footprint by sharing the processors and communication buffers Readers will benefit from the authors combined use of analytical models estimation methods and exploration algorithms and will be enabled to explore billions of design points in a few minutes *Customizable Embedded Processors* Paolo Ienne,Rainer Leupers,2006-08-30 Customizable processors have been described as the next natural step in the evolution of the microprocessor business a step in the life of a new technology where top performance alone is no longer sufficient to guarantee market success Other factors become fundamental such as time to market convenience energy efficiency and ease of customization This book is the first to explore comprehensively one of the most fundamental trends which emerged in the last decade to treat processors not as rigid fixed entities which designers include as is in their products but rather to build sound methodologies to tailor fit processors to the specific needs of such products This book addresses the goal of maintaining a very large family of processors with a wide range of features at a cost comparable to that of maintaining a single processor First book to present comprehensively the major ASIP design methodologies and tools without any particular bias Written by most of the pioneers and top international experts of this young domain Unique mix of management perspective technical detail research outlook and practical implementation Application Analysis Tools for Asip Design Kingshuk Karuri,Rainer Leupers,2011-06-01 *ESL Design and Verification* Grant Martin,Brian Bailey,Andrew Piziali,2010-07-27 Visit the authors companion site <http://www.electronicssystemlevel.com> Includes interactive forum with the authors Electronic System Level ESL design has mainstreamed it is now an established approach at most of the world s leading system on chip SoC design companies and is being used increasingly in system design From its genesis as an algorithm modeling methodology with no links to implementation ESL is evolving into a set of complementary methodologies that enable embedded system design verification and debug through to the hardware and software implementation of custom SoC system on FPGA system on board and entire multi board systems This book arises from experience the authors have gained from years of work as industry practitioners in the Electronic System Level design area they have seen SLD or ESL go through many stages and false starts and have observed that the shift in design methodologies to ESL is finally occurring This is partly because of ESL technologies themselves are stabilizing on a useful set of languages being standardized SystemC is the most notable and use models are being identified that are beginning to get real adoption ESL DESIGN VERIFICATION offers a true prescriptive guide to ESL that reviews its past and outlines the best practices of today Table of ContentsCHAPTER 1 WHAT IS ESL CHAPTER 2 TAXONOMY AND DEFINITIONS FOR THE ELECTRONIC SYSTEM LEVEL CHAPTER 3 EVOLUTION OF ESL DEVELOPMENT CHAPTER 4 WHAT ARE THE ENABLERS OF ESL CHAPTER 5 ESL FLOW CHAPTER 6 SPECIFICATIONS AND MODELING CHAPTER 7 PRE PARTITIONING ANALYSIS CHAPTER 8 PARTITIONING CHAPTER 9 POST PARTITIONING ANALYSIS AND DEBUG CHAPTER 10 POST PARTITIONING VERIFICATION CHAPTER 11 HARDWARE IMPLEMENTATION CHAPTER 12 SOFTWARE IMPLEMENTATION CHAPTER 13 USE OF ESL FOR

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