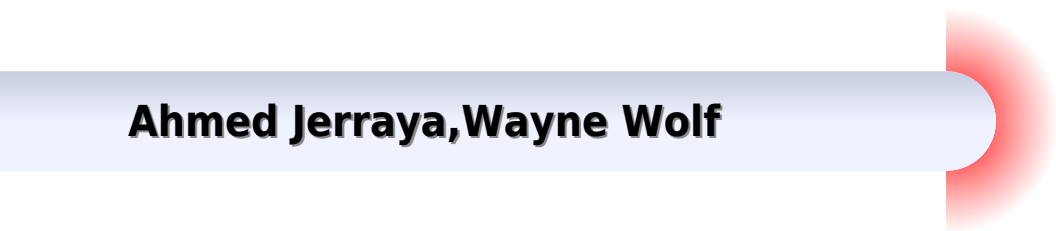


ASIC and FPGA Verification A Guide to Component Modeling First Edition Richard Munden



Asic And Fpga Verification A Guide To Component Modeling Systems On Silicon

Ahmed Jerraya, Wayne Wolf



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ASIC and FPGA Verification Richard Munden, 2004-10-23 Richard Munden demonstrates how to create and use simulation models for verifying ASIC and FPGA designs and board level designs that use off the shelf digital components Based on the VHDL VITAL standard these models include timing constraints and propagation delays that are required for accurate verification of today s digital designs **ASIC and FPGA Verification A Guide to Component Modeling** expertly illustrates how ASICs and FPGAs can be verified in the larger context of a board or a system It is a valuable resource for any designer who simulates multi chip digital designs Provides numerous models and a clearly defined methodology for performing board level simulation Covers the details of modeling for verification of both logic and timing First book to collect and teach techniques for using VHDL to model off the shelf or IP digital components for use in FPGA and board level design verification

System-on-Chip Test Architectures Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, 2010-07-28 Modern electronics testing has a legacy of more than 40 years The introduction of new technologies especially nanometer technologies with 90nm or smaller geometry has allowed the semiconductor industry to keep pace with the increased performance capacity demands from consumers As a result semiconductor test costs have been growing steadily and typically amount to 40% of today s overall product cost This book is a comprehensive guide to new VLSI Testing and Design for Testability techniques that will allow students researchers DFT practitioners and VLSI designers to master quickly System on Chip Test architectures for test debug and diagnosis of digital memory and analog mixed signal designs Emphasizes VLSI Test principles and Design for Testability architectures with numerous illustrations examples Most up to date coverage available including Fault Tolerance Low Power Testing Defect and Error Tolerance Network on Chip NOC Testing Software Based Self Testing FPGA Testing MEMS Testing and System In Package SIP Testing which are not yet available in any testing book Covers the entire spectrum of VLSI testing and DFT architectures from digital and analog to memory circuits and fault diagnosis and self repair from digital to memory circuits Discusses future nanotechnology test trends and challenges facing the nanometer design era promising nanotechnology test techniques including Quantum Dots Cellular Automata Carbon Nanotubes and Hybrid Semiconductor Nanowire Molecular Computing Practical problems at the end of each chapter for students

VLSI Test Principles and Architectures Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, 2006-08-14 This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product drive down test cost improve product quality and yield and speed up time to market and time to volume Most up to date coverage of design for testability Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books Numerous practical examples in each chapter illustrating basic VLSI test principles and DFT architectures

Verification Techniques for System-Level Design Masahiro Fujita, Indradeep Ghosh, Mukul Prasad, 2010-07-27 This book will explain how to verify SoC Systems on Chip logic designs using formal and semiformal

verification techniques The critical issue to be addressed is whether the functionality of the design is the one that the designers intended Simulation has been used for checking the correctness of SoC designs as in functional verification but many subtle design errors cannot be caught by simulation Recently formal verification giving mathematical proof of the correctness of designs has been gaining popularity For higher design productivity it is essential to debug designs as early as possible which this book facilitates This book covers all aspects of high level formal and semiformal verification techniques for system level designs First book that covers all aspects of formal and semiformal high level higher than RTL design verification targeting SoC designs Formal verification of high level designs RTL or higher Verification techniques are discussed with associated system level design methodology

On-Chip Communication Architectures Sudeep

Pasricha,Nikil Dutt,2010-07-28 Over the past decade system on chip SoC designs have evolved to address the ever increasing complexity of applications fueled by the era of digital convergence Improvements in process technology have effectively shrunk board level components so they can be integrated on a single chip New on chip communication architectures have been designed to support all inter component communication in a SoC design These communication architecture fabrics have a critical impact on the power consumption performance cost and design cycle time of modern SoC designs As application complexity strains the communication backbone of SoC designs academic and industrial R D efforts and dollars are increasingly focused on communication architecture design On Chip Communication Architectures is a comprehensive reference on concepts research and trends in on chip communication architecture design It will provide readers with a comprehensive survey not available elsewhere of all current standards for on chip communication architectures A definitive guide to on chip communication architectures explaining key concepts surveying research efforts and predicting future trends Detailed analysis of all popular standards for on chip communication architectures Comprehensive survey of all research on communication architectures covering a wide range of topics relevant to this area spanning the past several years and up to date with the most current research efforts Future trends that will have a significant impact on research and design of communication architectures over the next several years

Electronic Design Automation Laung-Terng

Wang,Yao-Wen Chang,Kwang-Ting (Tim) Cheng,2009-03-11 This book provides broad and comprehensive coverage of the entire EDA flow EDA VLSI practitioners and researchers in need of fluency in an adjacent field will find this an invaluable reference to the basic EDA concepts principles data structures algorithms and architectures for the design verification and test of VLSI circuits Anyone who needs to learn the concepts principles data structures algorithms and architectures of the EDA flow will benefit from this book Covers complete spectrum of the EDA flow from ESL design modeling to logic test synthesis verification physical design and test helps EDA newcomers to get up and running quickly Includes comprehensive coverage of EDA concepts principles data structures algorithms and architectures helps all readers improve their VLSI design competence Contains latest advancements not yet available in other books including Test compression ESL design

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Alexander, 2011-04-18 The steady and unabated increase in the capacity of silicon has brought the semiconductor industry to a watershed challenge. Now a single chip can integrate a radio transceiver, a network interface, multimedia functions, all the glue needed to hold it together, as well as a design that allows the hardware and software to be reconfigured for future applications. Such complex heterogeneous systems demand a different design methodology. A consortium of industrial and government labs have created a new language and a new design methodology to support this effort. Rosetta permits designers to specify requirements and constraints independent of their low level implementation and to integrate the designs of domains as distinct as digital and analog electronics and the mechanical, optical, fluidic and thermal subsystems with which they interact. In this book, Perry Alexander, one of the developers of Rosetta, provides a tutorial introduction to the language and the system level design methodology it was designed to support. The first commercially published book on this system level design language. Teaches you all you need to know on how to specify, define and generate models in Rosetta. A presentation of complete case studies analyzing design trade offs for power consumption, security requirements in a networking environment and constraints for hardware/software co design. Multiprocessor Systems-on-Chips Ahmed Jerraya, Wayne Wolf, 2005 Modern system on chip SoC design shows a clear trend toward integration of multiple processor cores on a single chip. Designing a multiprocessor system on chip MPSOC requires an understanding of the various design styles and techniques used in the multiprocessor. Understanding the application area of the MPSOC is also critical to making proper tradeoffs and design decisions. Multiprocessor Systems on Chips covers both design techniques and applications for MPSOCs. Design topics include multiprocessor architectures, processors, operating systems, compilers, methodologies and synthesis algorithms and application areas covered include telecommunications and multimedia. The majority of the chapters were collected from presentations made at the International Workshop on Application Specific Multi Processor SoC held over the past two years. The workshop assembled internationally recognized speakers on the range of topics relevant to MPSOCs. After having refined their material at the workshop, the speakers are now writing chapters and the editors are fashioning them into a unified book by making connections between chapters and developing common terminology. Examines several different architectures and the constraints imposed on them. Discusses scheduling real time operating systems and compilers. Analyzes design trade off and decisions in telecommunications and multimedia applications.

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