

Yongquan Fan
Zeljko Zilic

Accelerating Test, Validation and Debug of High Speed Serial Interfaces

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SA Adler



Accelerating Test Validation And Debug Of High Speed Serial Interfaces:

Accelerating Test, Validation and Debug of High Speed Serial Interfaces Yongquan Fan,Zeljko Zilic,2010-10-20 High Speed Serial Interface HSSI devices have become widespread in communications from the embedded to high performance computing systems and from on chip to a wide haul Testing of HSSIs has been a challenging topic because of signal integrity issues long test time and the need of expensive instruments Accelerating Test Validation and Debug of High Speed Serial Interfaces provides innovative test and debug approaches and detailed instructions on how to arrive to practical test of modern high speed interfaces Accelerating Test Validation and Debug of High Speed Serial Interfaces first proposes a new algorithm that enables us to perform receiver test more than 1000 times faster Then an under sampling based transmitter test scheme is presented The scheme can accurately extract the transmitter jitter and finish the whole transmitter test within 100ms while the test usually takes seconds The book also presents and external loopback based testing scheme where and FPGA based BER tester and a novel jitter injection technique are proposed These schemes can be applied to validate test and debug HSSIs with data rate up to 12.5Gbps at a lower test cost than pure ATE solutions In addition the book introduces an efficient scheme to implement high performance Gaussian noise generators suitable for evaluating BER performance under noise conditions

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An Engineer's Guide to Automated Testing of High-Speed Interfaces, Second Edition Jose Moreira,Hubert Werkmann,2016-04-30 This second edition of An Engineer's Guide to Automated Testing of High Speed Interfaces provides updates to reflect current state of the art high speed digital testing with automated test equipment technology ATE Featuring clear examples this one stop reference covers all critical aspects of automated testing including an introduction to high speed digital basics a discussion of industry

standards ATE and bench instrumentation for digital applications and test and measurement techniques for characterization and production environment Engineers learn how to apply automated test equipment for testing high speed digital I O interfaces and gain a better understanding of PCI Express 4 100Gb Ethernet and MIPI while exploring the correlation between phase noise and jitter This updated resource provides expanded material on 28 32 Gbps NRZ testing and wireless testing that are becoming increasingly more pertinent for future applications This book explores the current trend of merging high speed digital testing within the fields of photonic and wireless testing Accelerating Jitter and BER Qualifications of High Speed Serial Communication Interfaces Yongquan Fan,2009 *Electrical & Electronics Abstracts* ,1997 *PC Tech Journal* ,1987-11 *Efficient Test Methodologies for High-Speed Serial Links* Hong Dongwoo,Kwang-Ting Cheng,2010-05-05

Efficient Test Methodologies for High Speed Serial Links describes in detail several new and promising techniques for cost effectively testing high speed interfaces with a high test coverage One primary focus of Efficient Test Methodologies for High Speed Serial Links is on efficient testing methods for jitter and bit error rate BER which are widely used for quantifying the quality of a communication system Various analysis as well as experimental results are presented to demonstrate the validity of the presented techniques *Efficient Test Methodologies for High-Speed Serial Links* Dongwoo Hong,Kwang-Ting Cheng,2009-12-24

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