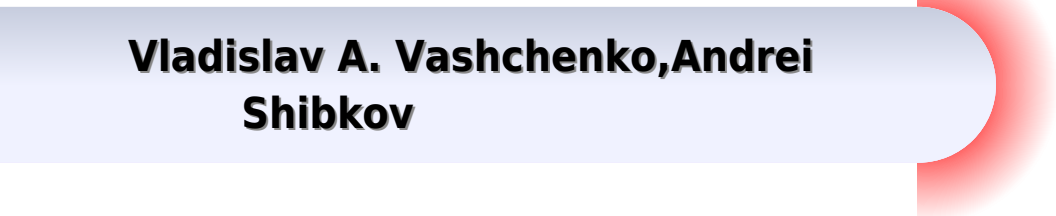


Basic ESD and I/O Design

Sanjay Dabral
Timothy J. Maloney

Basic Esd And Io Design

**Vladislav A. Vashchenko, Andrei
Shibkov**



Basic ESD And Io Design:

Basic ESD and I/O Design Sanjay Dabral, Timothy Maloney, 1998 This volume presents an integrated treatment of ESD I/O and process parameter interactions that both I/O designers and process designers can use. It examines key factors in I/O and ESD design and testing and helps the reader consider ESD and reliability issues up front when making I/O choices. Emphasizing clarity and simplicity, this book focuses on design principles that can be applied widely as this dynamic field continues to evolve.

Physical Design Essentials Khosrow Golshan, 2007-04-08 Arranged in a format that follows the industry common ASIC physical design flow, Physical Design Essentials begins with general concepts of an ASIC library, then examines floorplanning, placement, routing, verification, and finally testing. Among the topics covered are Basic standard cell design, transistor sizing, and layout styles. Linear, non-linear, and polynomial characterization, Physical design constraints, and floorplanning styles. Algorithms used for placement, Clock Tree Synthesis, Parasitic extraction, Electronic Testing, and many more.

ESD Protection Device and Circuit Design for Advanced CMOS Technologies Oleg Semenov, Hossein Sarbishaei, Manoj Sachdev, 2008-04-26 ESD Protection Device and Circuit Design for Advanced CMOS Technologies is intended for practicing engineers working in the areas of circuit design, VLSI reliability, and testing domains. As the problems associated with ESD failures and yield losses become significant in the modern semiconductor industry, the demand for graduates with a basic knowledge of ESD is also increasing. Today there is a significant demand to educate the circuits design and reliability teams on ESD issues. This book makes an attempt to address the ESD design and implementation in a systematic manner. A design procedure involving device simulators as well as circuit simulator is employed to optimize device and circuit parameters for optimal ESD as well as circuit performance. This methodology described in ESD Protection Device and Circuit Design for Advanced CMOS Technologies has resulted in several successful ESD circuit designs with excellent silicon results and demonstrates its strengths.

System Level ESD Co-Design Charvaka Duvvury, Harald Gossner, 2017-05-05 An effective and cost-efficient protection of electronic systems against ESD stress pulses specified by IEC 61000-4-2 is paramount for any system design. This pioneering book presents the collective knowledge of system designers and system testing experts and state-of-the-art techniques for achieving efficient system-level ESD protection with minimum impact on the system performance. All categories of system failures ranging from hard to soft types are considered to review simulation and tool applications that can be used. The principal focus of System Level ESD Co-Design is defining and establishing the importance of co-design efforts from both IC supplier and system builder perspectives. ESD designers often face challenges in meeting customers' system-level ESD requirements, and therefore a clear understanding of the techniques presented here will facilitate effective simulation approaches leading to better solutions without compromising system performance. With contributions from Robert Ashton, Jeffrey Dunnihoo, Micheal Hopkins, Pratik Maheshwari, David Pomerence, Wolfgang Reinprecht, and Matti Usumaki, readers benefit from hands-on experience and in-depth knowledge in topics ranging

from ESD design and the physics of system ESD phenomena to tools and techniques to address soft failures and strategies to design ESD robust systems that include mobile and automotive applications The first dedicated resource to system level ESD co design this is an essential reference for industry ESD designers system builders IC suppliers and customers and also Original Equipment Manufacturers OEMs Key features Clarifies the concept of system level ESD protection Introduces a co design approach for ESD robust systems Details soft and hard ESD fail mechanisms Detailed protection strategies for both mobile and automotive applications Explains simulation tools and methodology for system level ESD co design and overviews available test methods and standards Highlights economic benefits of system ESD co design High-Performance Energy-Efficient Microprocessor Design Vojin G. Oklobdzija, Ram K. Krishnamurthy, 2007-04-27 Microprocessors of today contain close to a billion transistors while achieving the performance of super computers just a decade ago Designing such processors takes hundreds of people organized into large teams High Performance Energy Efficient Microprocessor Design is written by the world s most prominent microprocessor design leaders from the industry and academia It provides a complete coverage of all the aspects of a complex microprocessor design process from technology power management clocking high performance architecture design methodologies memory and I O design computer aided design testing and design for testability The chapters are written to provide the latest state of the art knowledge of particular aspects of microprocessor design while including sufficient tutorial content in order to bring non experts up to speed High Performance Energy Efficient Microprocessor Design is intended to be a useful companion book for every design engineer working in the related areas and a source of technical information as well as a comprehensive reference in the field It should also serve as the source book for technical and business managers involved in microprocessor based design and manufacture The chapters are organized in a way which makes it possible to use this book as a textbook for graduate courses in advanced digital and system design The book is intended to highlight practical problems encountered in designing state of the art processors while yet covering fundamental principles that are independent of technology **Engineering the CMOS Library** David Doman, 2012-02-17 Shows readers how to gain the competitive edge in the integrated circuit marketplace This book offers a wholly unique perspective on the digital design kit It points to hidden value in the safety margins of standard cell libraries and shows design engineers and managers how to use this knowledge to beat the competition Engineering the CMOS Library reveals step by step how the generic foundry provided standard cell library is built and how to extract value from existing std cells and EDA tools in order to produce tighter margined smaller faster less power hungry and more yield producing integrated circuits It explores all aspects of the digital design kit including the different views of CMOS std cell libraries along with coverage of IO libraries memory compilers and small analog blocks Readers will learn How to work with overdesigned std cell libraries to improve profitability while maintaining safety How functions usually found in std cell libraries cover the design environment and how to add any missing functions How to harness the characterization technique

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