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# A Primer on Hardware Prefetching

**Babak Falsafi**

**Thomas F. Wenisch**

*SYNTHESIS LECTURES*  
*COMPUTER ARCHITECTURE*

Mark D. Hill, *Editor*

# A Primer On Hardware Prefetching Thomas F Wenisch

**Edouard Bugnion, Jason Nieh, Dan  
Tsafrir**



## **A Primer On Hardware Prefetching Thomas F Wenisch:**

*A Primer on Hardware Prefetching* Babak Falsafi, Thomas F. Wenisch, 2022-06-01 Since the 1970 s microprocessor based digital platforms have been riding Moore s law allowing for doubling of density for the same area roughly every two years However whereas microprocessor fabrication has focused on increasing instruction execution rate memory fabrication technologies have focused primarily on an increase in capacity with negligible increase in speed This divergent trend in performance between the processors and memory has led to a phenomenon referred to as the Memory Wall To overcome the memory wall designers have resorted to a hierarchy of cache memory levels which rely on the principal of memory access locality to reduce the observed memory access time and the performance gap between processors and memory Unfortunately important workload classes exhibit adverse memory access patterns that baffle the simple policies built into modern cache hierarchies to move instructions and data across cache levels As such processors often spend much time idling upon a demand fetch of memory blocks that miss in higher cache levels Prefetching predicting future memory accesses and issuing requests for the corresponding memory blocks in advance of explicit accesses is an effective approach to hide memory access latency There have been a myriad of proposed prefetching techniques and nearly every modern processor includes some hardware prefetching mechanisms targeting simple and regular memory access patterns This primer offers an overview of the various classes of hardware prefetchers for instructions and data proposed in the research literature and presents examples of techniques incorporated into modern microprocessors

*A Primer on Memory Persistency* Vaibhav Gogte, Aasheesh Kolli, Thomas F. Wenisch, 2022-06-01 This book introduces readers to emerging persistent memory PM technologies that promise the performance of dynamic random access memory DRAM with the durability of traditional storage media such as hard disks and solid state drives SSDs Persistent memories PMs such as Intel s Optane DC persistent memories are commercially available today Unlike traditional storage devices PMs can be accessed over a byte addressable load store interface with access latency that is comparable to DRAM Unfortunately existing hardware and software systems are ill equipped to fully avail the potential of these byte addressable memory technologies as they have been designed to access traditional storage media over a block based interface Several mechanisms have been explored in the research literature over the past decade to design hardware and software systems that provide high performance access to PMs Because PMs are durable they can retain data across failures such as power failures and program crashes Upon a failure recovery mechanisms may inspect PM data reconstruct state and resume program execution Correct recovery of data requires that operations to the PM are properly ordered during normal program execution Memory persistency models define the order in which memory operations are performed at the PM Much like memory consistency models memory persistency models may be relaxed to improve application performance Several proposals have emerged recently to design memory persistency models for hardware and software systems and for high level programming languages These proposals

differ in several key aspects they relax PM ordering constraints introduce varying programmability burden and introduce differing granularity of failure atomicity for PM operations This primer provides a detailed overview of the various classes of the memory persistency models their implementations in hardware programming languages and software systems proposed in the recent research literature and the PM ordering techniques employed by modern processors      **Research**

**Infrastructures for Hardware Accelerators** Yakun Sophia Shao,David Brooks,2022-05-31 Hardware acceleration in the form of customized datapath and control circuitry tuned to specific applications has gained popularity for its promise to utilize transistors more efficiently Historically the computer architecture community has focused on general purpose processors and extensive research infrastructure has been developed to support research efforts in this domain Envisioning future computing systems with a diverse set of general purpose cores and accelerators computer architects must add accelerator related research infrastructures to their toolboxes to explore future heterogeneous systems This book serves as a primer for the field as an overview of the vast literature on accelerator architectures and their design flows and as a resource guidebook for researchers working in related areas      *Hardware and Software Support for Virtualization* Edouard

Bugnion,Jason Nieh,Dan Tsafir,2022-06-01 This book focuses on the core question of the necessary architectural support provided by hardware to efficiently run virtual machines and of the corresponding design of the hypervisors that run them Virtualization is still possible when the instruction set architecture lacks such support but the hypervisor remains more complex and must rely on additional techniques Despite the focus on architectural support in current architectures some historical perspective is necessary to appropriately frame the problem The first half of the book provides the historical perspective of the theoretical framework developed four decades ago by Popek and Goldberg It also describes earlier systems that enabled virtualization despite the lack of architectural support in hardware As is often the case theory defines a necessary but not sufficient set of features and modern architectures are the result of the combination of the theoretical framework with insights derived from practical systems The second half of the book describes state of the art support for virtualization in both x86 64 and ARM processors This book includes an in depth description of the CPU memory and I O virtualization of these two processor architectures as well as case studies on the Linux KVM VMware and Xen hypervisors It concludes with a performance comparison of virtualization on current generation x86 and ARM based systems across multiple hypervisors      A Primer on Memory Consistency and Cache Coherence, Second Edition Vijay Nagarajan,Daniel J.

Sorin,Mark D. Hill,David A. Wood,2022-05-31 Many modern computer systems including homogeneous and heterogeneous architectures support shared memory in hardware In a shared memory system each of the processor cores may read and write to a single shared address space For a shared memory machine the memory consistency model defines the architecturally visible behavior of its memory system Consistency definitions provide rules about loads and stores or memory reads and writes and how they act upon memory As part of supporting a memory consistency model many machines also

provide cache coherence protocols that ensure that multiple cached copies of data are kept up to date The goal of this primer is to provide readers with a basic understanding of consistency and coherence This understanding includes both the issues that must be solved as well as a variety of solutions We present both high level concepts as well as specific concrete examples from real world systems This second edition reflects a decade of advancements since the first edition and includes among other more modest changes two new chapters one on consistency and coherence for non CPU accelerators with a focus on GPUs and one that points to formal work and tools on consistency and coherence

**A Primer on Compression in the Memory Hierarchy** Somayeh Sardashti, Angelos Arelakis, Per Stenström, David A. Wood, 2022-05-31 This synthesis lecture presents the current state of the art in applying low latency lossless hardware compression algorithms to cache memory and the memory cache link There are many non trivial challenges that must be addressed to make data compression work well in this context First since compressed data must be decompressed before it can be accessed decompression latency ends up on the critical memory access path This imposes a significant constraint on the choice of compression algorithms Second while conventional memory systems store fixed size entities like data types cache blocks and memory pages these entities will suddenly vary in size in a memory system that employs compression Dealing with variable size entities in a memory system using compression has a significant impact on the way caches are organized and how to manage the resources in main memory We systematically discuss solutions in the open literature to these problems Chapter 2 provides the foundations of data compression by first introducing the fundamental concept of value locality We then introduce a taxonomy of compression algorithms and show how previously proposed algorithms fit within that logical framework Chapter 3 discusses the different ways that cache memory systems can employ compression focusing on the trade offs between latency capacity and complexity of alternative ways to compact compressed cache blocks Chapter 4 discusses issues in applying data compression to main memory and Chapter 5 covers techniques for compressing data on the cache to memory links This book should help a skilled memory system designer understand the fundamental challenges in applying compression to the memory hierarchy and introduce him her to the state of the art techniques in addressing them

**iRODS Primer 2** Yu-Ting Chen, Jason Cong, Michael Gill, Glenn Reinman, Bingjun Xiao, Zhiyang Ong, 2015-07-01 Since the end of Dennard scaling in the early 2000s improving the energy efficiency of computation has been the main concern of the research community and industry The large energy efficiency gap between general purpose processors and application specific integrated circuits ASICs motivates the exploration of customizable architectures where one can adapt the architecture to the workload In this Synthesis lecture we present an overview and introduction of the recent developments on energy efficient customizable architectures including customizable cores and accelerators on chip memory customization and interconnect optimization In addition to a discussion of the general techniques and classification of different approaches used in each area we also highlight and illustrate some of the most successful design examples in each category and discuss their

impact on performance and energy efficiency We hope that this work captures the state of the art research and development on customizable architectures and serves as a useful reference basis for further research design and implementation for large scale deployment in future computing systems

**General-Purpose Graphics Processor Architectures** Tor M. Aamodt, Wilson Wai Lun Fung, Timothy G. Rogers, 2022-05-31 Originally developed to support video games graphics processor units GPUs are now increasingly used for general purpose non graphics applications ranging from machine learning to mining of cryptographic currencies GPUs can achieve improved performance and efficiency versus central processing units CPUs by dedicating a larger fraction of hardware resources to computation In addition their general purpose programmability makes contemporary GPUs appealing to software developers in comparison to domain specific accelerators This book provides an introduction to those interested in studying the architecture of GPUs that support general purpose computing It collects together information currently only found among a wide range of disparate sources The authors led development of the GPGPU Sim simulator widely used in academic research on GPU architectures The first chapter of this book describes the basic hardware structure of GPUs and provides a brief overview of their history Chapter 2 provides a summary of GPU programming models relevant to the rest of the book Chapter 3 explores the architecture of GPU compute cores Chapter 4 explores the architecture of the GPU memory system After describing the architecture of existing systems Chapters 3 and 4 provide an overview of related research Chapter 5 summarizes cross cutting research impacting both the compute core and memory system This book should provide a valuable resource for those wishing to understand the architecture of graphics processor units GPUs used for acceleration of general purpose applications and to those who want to obtain an introduction to the rapidly growing body of research exploring how to improve the architecture of these GPUs

**AI for Computer Architecture** Lizhong Chen, Drew Penney, Daniel Jiménez, 2022-05-31 Artificial intelligence has already enabled pivotal advances in diverse fields yet its impact on computer architecture has only just begun In particular recent work has explored broader application to the design optimization and simulation of computer architecture Notably machine learning based strategies often surpass prior state of the art analytical heuristic and human expert approaches This book reviews the application of machine learning in system wide simulation and run time optimization and in many individual components such as caches memories branch predictors networks on chip and GPUs The book further analyzes current practice to highlight useful design strategies and identify areas for future work based on optimized implementation strategies opportune extensions to existing work and ambitious long term possibilities Taken together these strategies and techniques present a promising future for increasingly automated computer architecture designs

**Robotic Computing on FPGAs** Shaoshan Liu, Zishen Wan, Bo Yu, Yu Wang, 2022-05-31 This book provides a thorough overview of the state of the art field programmable gate array FPGA based robotic computing accelerator designs and summarizes their adopted optimized techniques This book consists of ten chapters delving into the details of how FPGAs have been utilized in robotic perception

localization planning and multi robot collaboration tasks In addition to individual robotic tasks this book provides detailed descriptions of how FPGAs have been used in robotic products including commercial autonomous vehicles and space exploration robots

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