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Editors

Adaptive Techniques for Dynamic Processor Optimization

Theory and Practice

Adaptive Techniques For Dynamic Processor Optimization

Adaptive Techniques For Dynamic Processor Optimization

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Adaptive Techniques For Dynamic Processor Optimization Adaptive Techniques For Dynamic Processor Optimization:

Adaptive Techniques for Dynamic Processor Optimization Alice Wang, Samuel Naffziger, 2008-07-23 The integrated circuit has evolved tremendously in recent years as Moore's Law has enabled exponentially more devices and functionality to be packed onto a single piece of silicon. In some ways however these highly integrated circuits of which microprocessors are the flagship example have become victims of their own success. Despite dramatic reductions in the switching energy of the transistors these reductions have kept pace neither with the increased integration levels nor with the higher switching frequencies. In addition the atomic dimensions being utilized by these highly integrated processors have given rise to much higher levels of random and systematic variation which undercut the gains from process scaling that would otherwise be realized. So these factors the increasing impact of variation and the struggle to control power consumption have given rise to a tremendous amount of innovation in the area of adaptive techniques for dynamic processor optimization. The fundamental premise behind adaptive processor design is the recognition that variations in manufacturing and environment cause a statically configured operating point to be far too inefficient. Inefficient designs waste power and performance and will quickly be surpassed by more adaptive designs just as it happens in the biological realm. Organisms must adapt to survive and a similar trend is seen with processors those that are enabled to adapt to their environment will be far more competitive.

Wafer Level 3-D ICs Process Technology Chuan Seng Tan, Ronald J. Gutmann, L. Rafael Reif, 2009-06-29 Three dimensional 3D integration is clearly the simplest answer to most of the semiconductor industry's vexing problems heterogeneous integration and reductions of power form factor delay and even cost. Conceptually the power latency and form factor of a system with a fixed number of transistors all scale roughly linearly with the diameter of the smallest sphere enclosing frequently interacting devices. This clearly provides the fundamental motivation behind 3D technologies which vertically stack several strata of device and interconnect layers with high vertical interconnectivity. In addition the ability to vertically stack strata with divergent and even incompatible process flows provides for low cost and low parasitic integration of diverse technologies such as sensors energy scavengers nonvolatile memory dense memory fast memory processors and RF layers. These capabilities coupled with today's trends of increasing levels of integrated functionality lower power smaller form factor increasingly divergent process flows and functional diversification would seem to make 3D technologies a natural choice for most of the semiconductor industry. Since the concept of vertical integration of different strata has been around for over 20 years why aren't vertically stacked strata endemic to the semiconductor industry? The simple answer to this question is that in the past the 3D advantages while interesting were not necessary due to the tremendous opportunities offered by geometric scaling. In addition even when the global interconnect problem of high performance single core processors seemed insurmountable without innovations such as 3D alternative architectural solutions such as multicores could eff

tively delay but not eliminate the need for 3D CMOS

CMOSET 2010 Semiconductor Technologies Track Presentation Slides CMOS Emerging Technologies Research, Innovative Research and Applications in Next-Generation High Performance Computing Hassan, Qusay F., 2016-07-05 High performance computing HPC describes the use of connected computing units to perform complex tasks. It relies on parallelization techniques and algorithms to synchronize these disparate units in order to perform faster than a single processor could alone. Used in industries from medicine and research to military and higher education, this method of computing allows for users to complete complex data intensive tasks. This field has undergone many changes over the past decade and will continue to grow in popularity in the coming years. Innovative Research Applications in Next Generation High Performance Computing aims to address the future challenges, advances, and applications of HPC and related technologies. As the need for such processors increases, so does the importance of developing new ways to optimize the performance of these supercomputers. This timely publication provides comprehensive information for researchers, students in ICT programs, developers, military and government organizations, and business professionals.

Organic Field Effect Transistors Ioannis Kyriakidis, 2008-12-25 Organic Field Effect Transistors presents the state of the art in organic field effect transistors (OFETs) with a particular focus on the materials and techniques useful for making integrated circuits. The monograph begins with some general background on organic semiconductors, discusses the types of organic semiconductor materials suitable for making field effect transistors, the fabrication processes used to make integrated circuits, and appropriate methods for measurement and modeling. Organic Field Effect Transistors is written as a basic introduction to the subject for practitioners. It will also be of interest to researchers looking for references and techniques that are not part of their subject area or routine. A synthetic organic chemist, for example, who is interested in making OFETs may use the book more as a device design and characterization reference. A thin film processing electrical engineer, on the other hand, may be interested in the book to learn about what types of electron-carrying organic semiconductors may be worth trying and learning more about organic semiconductor physics.

Low Power Design Essentials Jan Rabaey, 2009-04-21 Low Power Design Essentials contains all the topics of importance to the low power designer. The book lays the foundation with background chapters entitled Advanced MOS Transistors and Their Models and Power Basics. These chapters are followed by chapters on the design process, including optimization, architecture, and algorithm level memory, run time, standby logic, and standby memory. Chapters on special topics are also included: power management and modal design, ultra low power, and low power design methodology and flows. The book concludes with a chapter on case studies as well as a chapter on Projection into the Future. These chapters are all based on the extensive amount of teaching that the author has carried out both at universities and companies worldwide. All chapters have been drawn up specifically for self study. They aim, however, at different levels of understanding. All the chapters start with elementary material but most also contain advanced material.

Embedded Memories for Nano-Scale VLSIs Kevin Zhang, 2009-04-21 Kevin Zhang, Advancement of semiconductor

technology has driven the rapid growth of very large scale integrated VLSI systems for increasingly broad applications including high end and mobile computing consumer electronics such as 3D gaming multi function or smart phone and various set top players and ubiquitous sensor and medical devices To meet the increasing demand for higher performance and lower power consumption in many different system applications it is often required to have a large amount of on die or embedded memory to support the need of data bandwidth in a system The varieties of embedded memory in a given system have also become increasingly more complex ranging from static to dynamic and volatile to nonvolatile Among embedded memories six transistor 6T based static random access memory SRAM continues to play a pivotal role in nearly all VLSI systems due to its superior speed and full compatibility with logic process technology But as the technology scaling continues SRAM design is facing severe challenge in maintaining sufficient cell stability margin under relentless area scaling Meanwhile rapid expansion in mobile application including new emerging application in sensor and medical devices requires far more aggressive voltage scaling to meet very stringent power constraint Many innovative circuit topologies and techniques have been extensively explored in recent years to address these challenges

Carbon Nanotube Electronics Ali Javey, Jing Kong, 2009-04-21 This book provides a complete overview of the field of carbon nanotube electronics It covers materials and physical properties synthesis and fabrication processes devices and circuits modeling and finally novel applications of nanotube based electronics The book introduces fundamental device physics and circuit concepts of 1 D electronics At the same time it provides specific examples of the state of the art nanotube devices

Applied Computational Fluid Dynamics Techniques Rainald Löhner, 2008-04-30 Computational fluid dynamics CFD is concerned with the efficient numerical solution of the partial differential equations that describe fluid dynamics CFD techniques are commonly used in the many areas of engineering where fluid behavior is an important factor Traditional fields of application include aerospace and automotive design and more recently bioengineering and consumer and medical electronics With *Applied Computational Fluid Dynamics Techniques* 2nd edition Rainald Löhner introduces the reader to the techniques required to achieve efficient CFD solvers forming a bridge between basic theoretical and algorithmic aspects of the finite element method and its use in an industrial context where methods have to be both as simple but also as robust as possible This heavily revised second edition takes a practice oriented approach with a strong emphasis on efficiency and offers important new and updated material on Overlapping and embedded grid methods Treatment of free surfaces Grid generation Optimal use of supercomputing hardware Optimal shape and process design *Applied Computational Fluid Dynamics Techniques* 2nd edition is a vital resource for engineers researchers and designers working on CFD aero and hydrodynamics simulations and bioengineering Its unique practical approach will also appeal to graduate students of fluid mechanics and aero and hydrodynamics as well as biofluidics

Multiprocessor System-on-Chip Michael Hübner, Jürgen Becker, 2010-11-25 The purpose of this book is to evaluate strategies for future system design in multiprocessor system on chip MPSoC architectures

Both hardware design and integration of new development tools will be discussed Novel trends in MPSoC design combined with reconfigurable architectures are a main topic of concern The main emphasis is on architectures design flow tool development applications and system design

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