

EXPERIEMENT NO. 1

Simulation using all the modeling styles and Synthesis of all the logic gates using Verilog HDL

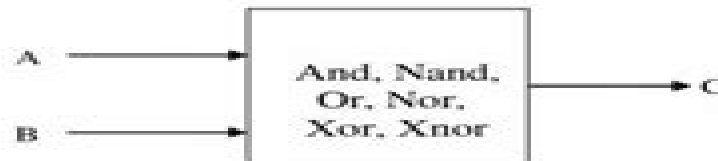
AIM:

Perform Zero Delay Simulation of all the logic gates written in behavioral, dataflow and structural modeling style in Verilog using a Test bench. then, Synthesize each one of them on two different EDA tools.

Electronics Design Automation Tools used:

- i) FPGA Advantage 3.1 (includes Model Sim simulation tool and Leonardo Spectrum Synthesis Tool)
- ii) Xilinx Project Navigator 8.1 (Includes all the steps in the design flow from Simulation to Implementation to download onto FPGA).

Block Diagram:



Truth table:

And Gate:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Nand Gate:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Xor Gate:

Or Gate:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Nor Gate:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Xnor Gate:

Arun Kumar Vhdl Lab Manual

Mike Jess



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Digital Electronics Lab Manual with Vhdl Scott Stewart, 2004-11-30 Programming Digital Applications W/Able, Vhdl-Lab Manual Han-Way Huang, 2006-07 **Digital Fundamentals with Cplds, Fpgas and Vhdl Laboratory Manual** David Buchla, Douglas Joks, 2002-09-30 A Guide to VHDL Stanley Mazor, Patricia Langstraat, 2013-06-29

A Guide to VHDL is intended for the working engineer who needs to develop document simulate and synthesize a design using the VHDL language It is for system and chip designers who are working with VHDL CAD tools and who have some experience programming in Fortran Pascal or C and have used a logic simulator A Guide to VHDL includes a number of paper exercises and computer lab experiments If a compiler simulator is available to the reader then the lab exercises included in the chapters can be run to reinforce the learning experience For practical purposes this book keeps simulator specific text to a minimum but does use the Synopsys VHDL Simulator command language in a few cases A Guide to VHDL can be used as a primer since its contents are appropriate for an introductory course in VHDL

The Student's Guide to VHDL Peter J. Ashenden, 2008-07-01 The Student's Guide to VHDL is a condensed edition of The Designer's Guide to VHDL the most widely used textbook on VHDL for digital system modeling The Student's Guide is targeted as a supplemental reference book for computer organization and digital design courses Since publication of the first edition of The Student's Guide the IEEE VHDL and related standards have been revised The Designer's Guide has been revised to reflect the changes so it is appropriate that The Student's Guide also be revised In The Student's Guide to VHDL 2nd Edition we have included a design case study illustrating an FPGA based design flow The aim is to show how VHDL modeling fits into a design flow starting from high level design and proceeding through detailed design and verification synthesis FPGA place and route and final timing verification Inclusion of the case study helps to better serve the educational market Currently most college courses do not formally address the details of design flow Students may be given informal guidance on how to proceed with lab projects In many cases it is left to students to work it out for themselves The case study in The Student's Guide provides a reference design flow that can be adapted to a variety of lab projects

The Designer's Guide to VHDL Peter J. Ashenden, 2002 CD ROM contains Access to an introductory version of a graphical VHDL simulator debugger from FTL Systems Code for examples and case studies

Introduction to VHDL R.D. Hunter, T. T. Johnson, 1996 Covers all aspects of the VHDL language

The VHDL Handbook David R. Coelho, 1989-06-30 This book is intended to be a working reference for electronic hardware designers who are interested in writing VHDL models A handbook cookbook approach is taken with many complete examples used to illustrate the features of the VHDL language and to provide insight into how particular classes of hardware devices can be modelled in VHDL It is possible to use these models directly or to adapt them to similar problems with minimal effort This book is not intended to be a complete reference manual for the VHDL language It is possible to begin writing VHDL models with little background in VHDL by copying examples from the book and adapting them to

particular problems Some exposure to the VHDL language prior to using this book is recommended The reader is assumed to have a solid hardware design background preferably with some simulation experience For the reader who is interested in getting a complete overview of the VHDL language the following publications are recommended reading An Introduction to VHDL Hardware Description and Design LIP89 IEEE Standard VHDL Language Reference Manual IEEE87 Chip Level Behavioral Modelling ARMS88 Multi Level Simulation of VLSI Systems COEL87 Other references of interest are USG88 DOD88 and CLSI87 Use of the Book If the reader is familiar with VHDL the models described in chapters 3 through 7 can be applied directly to design problems Introduction to VHDL ,1997 VHDL: Programming by Example Douglas L. Perry,2002-06-02 Teaches VHDL by example Includes tools for simulation and synthesis CD ROM containing Code Design examples and a working demo of ModelSIM

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Table of Contents Arun Kumar Vhdl Lab Manual

1. Understanding the eBook Arun Kumar Vhdl Lab Manual
 - The Rise of Digital Reading Arun Kumar Vhdl Lab Manual
 - Advantages of eBooks Over Traditional Books
2. Identifying Arun Kumar Vhdl Lab Manual
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Arun Kumar Vhdl Lab Manual
 - User-Friendly Interface
4. Exploring eBook Recommendations from Arun Kumar Vhdl Lab Manual
 - Personalized Recommendations
 - Arun Kumar Vhdl Lab Manual User Reviews and Ratings
 - Arun Kumar Vhdl Lab Manual and Bestseller Lists

5. Accessing Arun Kumar Vhdl Lab Manual Free and Paid eBooks
 - Arun Kumar Vhdl Lab Manual Public Domain eBooks
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 - Arun Kumar Vhdl Lab Manual Budget-Friendly Options
6. Navigating Arun Kumar Vhdl Lab Manual eBook Formats
 - ePub, PDF, MOBI, and More
 - Arun Kumar Vhdl Lab Manual Compatibility with Devices
 - Arun Kumar Vhdl Lab Manual Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Arun Kumar Vhdl Lab Manual
 - Highlighting and Note-Taking Arun Kumar Vhdl Lab Manual
 - Interactive Elements Arun Kumar Vhdl Lab Manual
8. Staying Engaged with Arun Kumar Vhdl Lab Manual
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Arun Kumar Vhdl Lab Manual
9. Balancing eBooks and Physical Books Arun Kumar Vhdl Lab Manual
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Arun Kumar Vhdl Lab Manual
10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
11. Cultivating a Reading Routine Arun Kumar Vhdl Lab Manual
 - Setting Reading Goals Arun Kumar Vhdl Lab Manual
 - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Arun Kumar Vhdl Lab Manual
 - Fact-Checking eBook Content of Arun Kumar Vhdl Lab Manual
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning

- Utilizing eBooks for Skill Development
- Exploring Educational eBooks

14. Embracing eBook Trends

- Integration of Multimedia Elements
- Interactive and Gamified eBooks

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