

Yongquan Fan
Zeljko Zilic

Accelerating Test, Validation and Debug of High Speed Serial Interfaces

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Hong Dongwoo, Kwang-Ting Cheng



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Accelerating Test, Validation and Debug of High Speed Serial Interfaces Yongquan Fan,Zeljko Zilic,2010-10-20 High Speed Serial Interface HSSI devices have become widespread in communications from the embedded to high performance computing systems and from on chip to a wide haul Testing of HSSIs has been a challenging topic because of signal integrity issues long test time and the need of expensive instruments Accelerating Test Validation and Debug of High Speed Serial Interfaces provides innovative test and debug approaches and detailed instructions on how to arrive to practical test of modern high speed interfaces Accelerating Test Validation and Debug of High Speed Serial Interfaces first proposes a new algorithm that enables us to perform receiver test more than 1000 times faster Then an under sampling based transmitter test scheme is presented The scheme can accurately extract the transmitter jitter and finish the whole transmitter test within 100ms while the test usually takes seconds The book also presents and external loopback based testing scheme where and FPGA based BER tester and a novel jitter injection technique are proposed These schemes can be applied to validate test and debug HSSIs with data rate up to 12.5Gbps at a lower test cost than pure ATE solutions In addition the book introduces an efficient scheme to implement high performance Gaussian noise generators suitable for evaluating BER performance under noise conditions

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An Engineer's Guide to Automated Testing of High-Speed Interfaces, Second Edition Jose Moreira,Hubert Werkmann,2016-04-30 This second edition of An Engineer's Guide to Automated Testing of High Speed Interfaces provides updates to reflect current state of the art high speed digital testing with automated test equipment technology ATE Featuring clear examples this one stop reference covers all critical aspects of automated testing including an introduction to high speed digital basics a discussion of industry

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Efficient Test Methodologies for High Speed Serial Links describes in detail several new and promising techniques for cost effectively testing high speed interfaces with a high test coverage One primary focus of Efficient Test Methodologies for High Speed Serial Links is on efficient testing methods for jitter and bit error rate BER which are widely used for quantifying the quality of a communication system Various analysis as well as experimental results are presented to demonstrate the validity of the presented techniques *Efficient Test Methodologies for High-Speed Serial Links* Dongwoo Hong,Kwang-Ting Cheng,2009-12-24

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Table of Contents Accelerating Test Validation And Debug Of High Speed Serial Interfaces

1. Understanding the eBook Accelerating Test Validation And Debug Of High Speed Serial Interfaces
 - The Rise of Digital Reading Accelerating Test Validation And Debug Of High Speed Serial Interfaces
 - Advantages of eBooks Over Traditional Books
2. Identifying Accelerating Test Validation And Debug Of High Speed Serial Interfaces
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Accelerating Test Validation And Debug Of High Speed Serial Interfaces
 - User-Friendly Interface
4. Exploring eBook Recommendations from Accelerating Test Validation And Debug Of High Speed Serial Interfaces
 - Personalized Recommendations
 - Accelerating Test Validation And Debug Of High Speed Serial Interfaces User Reviews and Ratings
 - Accelerating Test Validation And Debug Of High Speed Serial Interfaces and Bestseller Lists
5. Accessing Accelerating Test Validation And Debug Of High Speed Serial Interfaces Free and Paid eBooks
 - Accelerating Test Validation And Debug Of High Speed Serial Interfaces Public Domain eBooks
 - Accelerating Test Validation And Debug Of High Speed Serial Interfaces eBook Subscription Services
 - Accelerating Test Validation And Debug Of High Speed Serial Interfaces Budget-Friendly Options

6. Navigating Accelerating Test Validation And Debug Of High Speed Serial Interfaces eBook Formats
 - ePub, PDF, MOBI, and More
 - Accelerating Test Validation And Debug Of High Speed Serial Interfaces Compatibility with Devices
 - Accelerating Test Validation And Debug Of High Speed Serial Interfaces Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Accelerating Test Validation And Debug Of High Speed Serial Interfaces
 - Highlighting and Note-Taking Accelerating Test Validation And Debug Of High Speed Serial Interfaces
 - Interactive Elements Accelerating Test Validation And Debug Of High Speed Serial Interfaces
8. Staying Engaged with Accelerating Test Validation And Debug Of High Speed Serial Interfaces
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Accelerating Test Validation And Debug Of High Speed Serial Interfaces
9. Balancing eBooks and Physical Books Accelerating Test Validation And Debug Of High Speed Serial Interfaces
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Accelerating Test Validation And Debug Of High Speed Serial Interfaces
10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
11. Cultivating a Reading Routine Accelerating Test Validation And Debug Of High Speed Serial Interfaces
 - Setting Reading Goals Accelerating Test Validation And Debug Of High Speed Serial Interfaces
 - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Accelerating Test Validation And Debug Of High Speed Serial Interfaces
 - Fact-Checking eBook Content of Accelerating Test Validation And Debug Of High Speed Serial Interfaces
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
 - Integration of Multimedia Elements

- Interactive and Gamified eBooks

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