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Analysis and Design of Networks-on-Chip under High Process Variation



Analysis Design Networks Process Variation

Ioannis Dritsas

Analysis Design Networks Process Variation:

Designing Network On-Chip Architectures in the Nanoscale Era Jose Flich, Davide Bertozzi, 2010-12-18 Going beyond isolated research ideas and design experiences Designing Network On Chip Architectures in the Nanoscale Era covers the foundations and design methods of network on chip NoC technology The contributors draw on their own lessons learned to provide strong practical guidance on various design issues Exploring the design process of the **Process Variations and Probabilistic Integrated Circuit Design** Manfred Dietrich, Joachim Haase, 2011-11-20 Uncertainty in key parameters within a chip and between different chips in the deep sub micron area plays a more and more important role As a result manufacturing process spreads need to be considered during the design process Quantitative methodology is needed to ensure faultless functionality despite existing process variations within given bounds during product development This book presents the technological physical and mathematical fundamentals for a design paradigm shift from a deterministic process to a probability orientated design process for microelectronic circuits Readers will learn to evaluate the different sources of variations in the design flow in order to establish different design variants while applying appropriate methods and tools to Network-on-Chip Architectures Chrysostomos Nicopoulos, Vijaykrishnan evaluate and optimize their design Narayanan, Chita R. Das, 2009-09-18 2 The Cell Processor from Sony Toshiba and IBM STI 3 and the Sun UltraSPARC T1 formerly codenamed Niagara 4 signal the growing popularity of such systems Furthermore Intel's very recently announced 80 core TeraFLOP chip 5 exemplifies the irreversible march toward many core systems with tens or even hundreds of processing elements 1 2 The Dawn of the Communication Centric Revolution The multi core thrust has ushered the gradual displacement of the computati centric design model by a more communication centric approach 6 The large sophisticated monolithic modules are giving way to several smaller simpler p cessing elements working in tandem This trend has led to a surge in the popularity of multi core systems which typically manifest themselves in two distinct incarnations heterogeneous Multi Processor Systems on Chip MPSoC and homogeneous Chip Multi Processors CMP The SoC philosophy revolves around the technique of Platform Based Design PBD 7 which advocates the reuse of Intellectual Property IP cores in flexible design templates that can be customized accordingly to satisfy the demands of particular implementations. The appeal of such a modular approach lies in the substantially reduced Time To Market TTM incubation period which is a direct outcome of lower circuit complexity and reduced design effort The whole system can now be viewed as a diverse collection of pre existing IP components integrated on a single die Nanoscale VLSI Rohit Dhiman, Rajeevan Chandel, 2020-10-03 This book describes methodologies in the design of VLSI devices circuits and their applications at nanoscale levels. The book begins with the discussion on the dominant role of power dissipation in highly scaled devices The 15 Chapters of the book are classified under four sections that cover design modeling and simulation of electronic magnetic and compound semiconductors for their applications in VLSI devices circuits and systems This comprehensive volume eloquently presents the design

methodologies for ultra low power VLSI design potential post CMOS devices and their applications from the architectural and system perspectives The book shall serve as an invaluable reference book for the graduate students Ph D M S M Tech Scholars researchers and practicing engineers working in the frontier areas of nanoscale VLSI design <u>Performance of Nanometer Digital Circuits Under Process Variations</u> Victor Champac, Jose Garcia Gervacio, 2018-04-18 This book discusses the digital design of integrated circuits under process variations with a focus on design time solutions. The authors describe a step by step methodology going from logic gates to logic paths to the circuit level Topics are presented in comprehensively without overwhelming use of analytical formulations Emphasis is placed on providing digital designers with understanding of the sources of process variations their impact on circuit performance and tools for improving their designs to comply with product specifications Various circuit level design hints are highlighted so that readers can use then to improve their designs A special treatment is devoted to unique design issues and the impact of process variations on the performance of FinFET based circuits This book enables readers to make optimal decisions at design time toward more efficient circuits with better yield and higher reliability **Stochastic Process Variation in Deep-Submicron CMOS** Amir Zjajo, 2013-11-19 One of the most notable features of nanometer scale CMOS technology is the increasing magnitude of variability of the key device parameters affecting performance of integrated circuits The growth of variability can be attributed to multiple factors including the difficulty of manufacturing control the emergence of new systematic variation generating mechanisms and most importantly the increase in atomic scale randomness where device operation must be described as a stochastic process In addition to wide sense stationary stochastic device variability and temperature variation existence of non stationary stochastic electrical noise associated with fundamental processes in integrated circuit devices represents an elementary limit on the performance of electronic circuits In an attempt to address these issues Stochastic Process Variation in Deep Submicron CMOS Circuits and Algorithms offers unique combination of mathematical treatment of random process variation electrical noise and temperature and necessary circuit realizations for on chip monitoring and performance calibration The associated problems are addressed at various abstraction levels i e circuit level architecture level and system level It therefore provides a broad view on the various solutions that have to be used and their possible combination in very effective complementary techniques for both analog mixed signal and digital circuits The feasibility of the described algorithms and built in circuitry has been verified by measurements from the silicon prototypes fabricated in standard 90 nm and 65 nm CMOS technology **Stochastic Optimization** Ioannis Dritsas, 2011-02-28 Stochastic Optimization Algorithms have become essential tools in solving a wide range of difficult and critical optimization problems Such methods are able to find the optimum solution of a problem with uncertain elements or to algorithmically incorporate uncertainty to solve a deterministic problem They even succeed in fighting uncertainty with uncertainty This book discusses theoretical aspects of many such algorithms and covers their application in various scientific fields **Emerging**

Electronics and Automation Peter Han Joo Chong, Akhtar Kalam, Antonio Pascoal, Manas Kumar Bera, 2022-11-09 This book constitutes peer reviewed proceedings of the International Conference on Emerging Electronics and Automation E2A 2021 The book presents new ideas research findings and novel techniques in the fields of sensors and instrumentation automation and control artificial intelligence MEMS sensors soft computing signal processing and communication It includes contributions received from both academia and industry The proceedings will be helpful for beginners as well as advanced **Model-Based Tools for Pharmaceutical Manufacturing** researchers in the area of automation and other allied fields Processes Krist V. Gernaey, René Schenkendorf, Dimitrios I. Gerogiorgis, Seyed Soheil Mansouri, 2020-03-13 The Special Issue on Model Based Tools for Pharmaceutical Manufacturing Processes will curate novel advances in the development and application of model based tools to address ever present challenges of the traditional pharmaceutical manufacturing practice as well as new trends This book provides a collection of nine papers on original advances in the model based process unit system level quality by design under uncertainty and decision making applications of pharmaceutical manufacturing Progress in Industrial Mathematics at ECMI 2014 Giovanni Russo, Vincenzo Capasso, Giuseppe Nicosia, Vittorio processes Romano, 2017-09-04 This book presents a collection of papers emphasizing applications of mathematical models and methods to real world problems of relevance for industry life science environment finance and so on The biannual Conference of ECMI the European Consortium of Mathematics in Industry held in 2014 focused on various aspects of industrial and applied mathematics The five main topics addressed at the conference were mathematical models in life science material science and semiconductors mathematical methods in the environment design automation and industrial applications and computational finance Several other topics have been treated such as among others optimization and inverse problems education numerical methods for stiff pdes model reduction imaging processing multi physics simulation mathematical models in textile industry The conference which brought together applied mathematicians and experts from industry provided a unique opportunity to exchange ideas problems and methodologies bridging the gap between mathematics and industry and contributing to the advancement of science and technology The conference has included a presentation of EU Maths In European Network of Mathematics for Industry and Innovation a recent joint initiative of ECMI and EMS The proceedings from this conference represent a snapshot of the current activity in industrial mathematics in Europe and are highly relevant to anybody interested in the latest applications of mathematics to industrial problems

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