#### EXPERIEMENT NO. 1

Simulation using all the modeling styles and Synthesis of all the logic gates using Verilog HDL

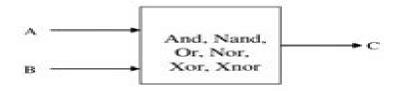
#### AIM:

Perform Zero Delay Simulation of all the logic gates written in behavioral, dataflow and structural modeling style in Verilog using a Test bench, then, Synthesize each one of them on two different EDA tools.

#### Electronics Design Automation Tools used:

- i) FPGA Advantage 3.1 (includes Model Sim simulation tool and Leonardo Spectrum Synthesis Tool)
- Xilinx Project Navigator 8.1 (Includes all the steps in the design flow from Simulation to Implementation to download onto FPGA).

#### Block Diagram:



## Truth table:

And Gate:

A	B	Y
0	0	-0
0	1	0
1.	0	0
1	1	1.

	The second secon
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	THE RESIDENCE OF THE PARTY OF

A	B	Y	
0	0	1	
0	1		
1	0	1	
1	1	0	Т

Xor Gate:

Or Gate:

A	В	Y
0	0	0
0.	1	1
1	0	1.1
110	1.	1

Nor Gate:

Ac	В	Y
0	0	1
0	1	0
1	0	0
100	1	0

Xnor Gate:

# **Arun Kumar Vhdl Lab Manual**

Peter J. Ashenden

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